WHAT IS CLAIMED IS:

1. A differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying said input voltage into an output voltage, and outputting said output voltage, wherein said range comprises a first range portion and a second range portion, and said input voltage ranged in said first range portion is higher than that ranged in said second range portion, comprising:

a first differential comparator for receiving and amplifying said input voltage within said first range portion, and outputting said output voltage;

a detecting circuit electrically connected to said first differential comparator for producing a trigger signal when said detecting circuit detects that said first differential comparator is shut down due to the fact that said input voltage is lower than a lower-limit of said first range portion; and

a second differential comparator electrically connected to said detecting circuit for receiving and amplifying said input voltage within said second range portion, and outputting said output voltage in response to said trigger signal.

2. The circuit according to Claim 1, wherein said differential comparator circuit is employed in a transmitting terminal of a Universal Serial Bus (USB).

3. The circuit according to Claim 1, wherein said first differential comparator further comprises:

a first differential receiving circuit for receiving said input voltage within said first range portion; and

a first operational amplifier circuit electrically connected to said first differential receiving circuit for amplifying said input voltage received by said first differential receiving circuit and generating said output voltage.

4. The circuit according to Claim 1, wherein said second differential comparator further comprises:

a second differential receiving circuit electrically connected to said detecting circuit for receiving said input voltage ranged in said second range portion in response to said trigger signal; and

a second operational amplifier circuit electrically connected to said second differential receiving circuit for amplifying said input voltage received by said second differential receiving circuit and generating said output voltage.

5. The circuit according to Claim 1, further comprising an output circuit for outputting said output voltage.

6. The circuit according to Claim 1, wherein said second differential comparator is shut down to avoid a floating when said first differential comparator is operated.

7. The circuit according to Claim 1, wherein said first differential comparator is shut down when said second differential comparator is operated.

8. A differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying said input voltage into an output voltage, and outputting said output voltage, wherein said range comprises a first range portion and a second range portion, and said input voltage ranged in said first range portion is higher than that ranged in said second range portion, comprising:

a first differential receiving circuit for receiving said input voltage ranged in said first range portion;

a first operational amplifier circuit electrically connected to said first differential receiving circuit for amplifying said input voltage received by said first differential receiving circuit and generating said output voltage;

a detecting circuit electrically connected to said first differential receiving circuit for producing a trigger signal when said detecting circuit detects said first differential receiving circuit is shut down due to the fact that said input voltage is lower than a lower-limit of said first range portion;

a second differential receiving circuit electrically connected to said detecting circuit for receiving said input voltage ranged in said second range portion in response to said trigger signal; and

a second operational amplifier circuit electrically connected to said second differential receiving circuit for amplifying said input voltage received by said second differential receiving circuit and generating said output voltage.

9. The circuit according to Claim 8, further comprising an output circuit for outputting said output voltage.

10. The circuit according to Claim 8, wherein said second differential receiving circuit is shut down to avoid a floating when said first differential receiving circuit and said first operational amplifier circuit are operated.

11. The circuit according to Claim 8, wherein said first differential receiving circuit and said first operational amplifier circuit are shut down when said second differential receiving circuit and said second operational amplifier circuit are operated.

12. A differential comparator circuit for receiving an input voltage within a pre-determined range, amplifying said input voltage into an output voltage, and outputting said output voltage, wherein said range comprises a first range portion and a second range portion, and said input voltage ranged in said first portion is higher than that ranged in said second range portion, comprising:

a first differential receiving circuit for receiving said input voltage ranged in said first range portion;

a detecting circuit electrically connected to said first differential receiving circuit for producing a trigger signal when said detecting circuit detects that said first differential receiving circuit is shut down due to the fact that said input voltage is lower than a lower-limit of said first range portion; and

a second differential receiving circuit electrically connected to said detecting circuit for receiving said input voltage ranged in said second range portion in response to said trigger signal.